



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/821,044

04/08/2004

Robert Allan Faust

AUS920040056US1

9661

35525 7590 04/12/2007
IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER

NGUYEN, VINH P

ART UNIT

PAPER NUMBER

2829

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
--	-----------	---------------

3 MONTHS

04/12/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/821,044

Applicant(s)

FAUST, ROBERT ALLAN

Examiner

VINH P. NGUYEN

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

1. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear what is meant by “indicating logic ones using first pulses that are a first width... and indicating logic zeros...” and what device is used for performing this step.

In claims 3 and 5, it is unclear how the step of “generating said first and second pulses...” are interrelated and associated with the step of indicating logical ones... and indicating logical zeros...” as recited in claim 1.

In claim 6, it is unclear how the step of “generating said first pulses...” and the step of “generating second pulses...” are interrelated and associated with the step of indicating logical ones... and indicating logical zeros...” as recited in claim 1.

In claims 10 and 19, it is unclear which device is used for “indicating” logic ones or logical zero.

In claim 12, it is unclear how “first and second pulses being generated using an external device” is interrelated and associated with the logical ones being indicated ... and logical zeros being indicated ...” as recited in claim 10.

In claim 15, it is unclear how “first pulses generated by closing said switch for a first length of time” and “second pulses generated by closing said switch for a second length of time” are interrelated and associated with “logic ones being indicated using first pulses that are a first width and logical zeros being indicated using second pulses that are a second width” as recited in claim 10.

In claim 18, it is unclear how "first and second pulses being generated using an external device" is interrelated and associated with the logical ones being indicated ... and logical zeros being indicated ..." as recited in claim 10.

In claim 20, it is unclear how "instructions for generating said first pulses..." and "instructions for generating second pulses..." are interrelated and associated with "instruction for indicating logical ones...a second length" as recited in claim 10.

The dependent claims not specifically address share the same indefiniteness as they depend from rejected base claims.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1,3,8-10,12 and 19 are rejected under 35 U.S.C. 102(a) as being anticipated by Frankowsky (Pat # 6,651,203).

As to claims 1, 10,12, Frankowsky discloses an apparatus for testing the memory device (102) with a plurality of I/O pins (DQ) as shown in figure 2 having at least one input/output pin (DQ) configured to be used to transmit and receive pulses, an external device (, 110,108) for communicating with the device (102) utilizing logic signal (one "high" or low "zero") (see

column 4, lines 20-31) by transmitting the logic signal to the device utilizing the I/O pin (DQ). It appears that the logical ones (high) in the device of Frankowsky inherently use pulses that are a first length and a logical zeros (low) in the device of Frankowsky inherently use pulses that are a second length.

As to claim 3, the external device (108,110) of Frankowsky is used for generating the logical ones and logical zeros and it is Coupled to the device (102) using the I/O pin (DQ).

As to claim 8, it appears that the external tester (110) of the external device (108,110) inherently includes a bidirectional driver in order to transmit and receive the signals from the device under test (102) and a first node (any output terminals of the tester "110") connected to that bidirectional driver and is also connected to a first communication pin (one of the terminals labeled as "data out") of the external device (108,110).

As to claim 9, the logical ones and zeros are generated by the external device (108,110) and outputted them using the first communication pin (one of the terminals labeled as "data out").

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

6. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Prysby et al. (Pat # 6,191,626) in view of Kim et al (Pat # c6,977,634).

As to claims 1,10 and 19, Prysby et al disclose an apparatus as shown in figure 1 having a device (RC), an I/O pin (25) to be used to transmit and receive pulses and Pulse width modulator (PWM) for generating pulses. According to Prysby et al, I/O pin (25) is configured/instructed to be used to transmit and receive the pulses from the Pulse width modulator (PWM) and communicating with the device (RC) by transmitting and receiving the pulses. Prysby et al do not mention about the logic ones using first pulses that are a first width and logical zeros using second pulses that are a second width.

Kim et al teach disclose a Pulse width modulation signal as shown in figure 3. From figure # 3, the logic ones (represents by "1" or "4" or "128") that uses first pulses that are a first width and logical zeros (signal between logic ones) that uses second pulses that are a second width (no width).

It would have been well known that the pulse width modulation signals of Prysby et al are the same as pulse width modulation signals as taught by Kim et al .

As to claims 3 and 12, the first and second pulses are generated by an external device (PWM) located outside of the RC circuit.

7. Applicant's arguments with respect to claims 1,3,8-10,12 and 19 filed on 01/29/07 have been considered but are moot in view of the new ground(s) of rejection.

Applicants' argued that Frankowsky teaches that each pulses that have different widths.

However, Examiner indicates that the logical ones (high) in the device of Frankowsky inherently use pulses that are a first width and a logical zeros (low) in the device of Frankowsky inherently use pulses that are a second length (no width). It appears that the claims do not call for the logic ones and the logic zeros are generated simultaneously. Therefore, the rejections of the instant claims over Frankowsky are still valid.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

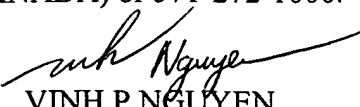
Lys et al (Pat # 7,113,541) disclose method for software driven generation of multiple simultaneous high speed pulse width modulated signals.

You et al (PG Pub No. 2006/029444A1) disclose an apparatus and method for testing PS/2 interface.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HA T. NGUYEN can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


VINH P NGUYEN
Primary Examiner
Art Unit 2829

04/09/07